

**CME2003 Logic Design**

**Experiment 6**



December 23, 2016

Dokuz eylul unıvercıty

Faculty of Engineering

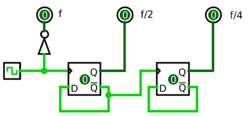
IZMIR / TURKEY

**GÜL EDA AYDEMİR**

**2015510013**

**Question 1:** Frequency Divider Circuit

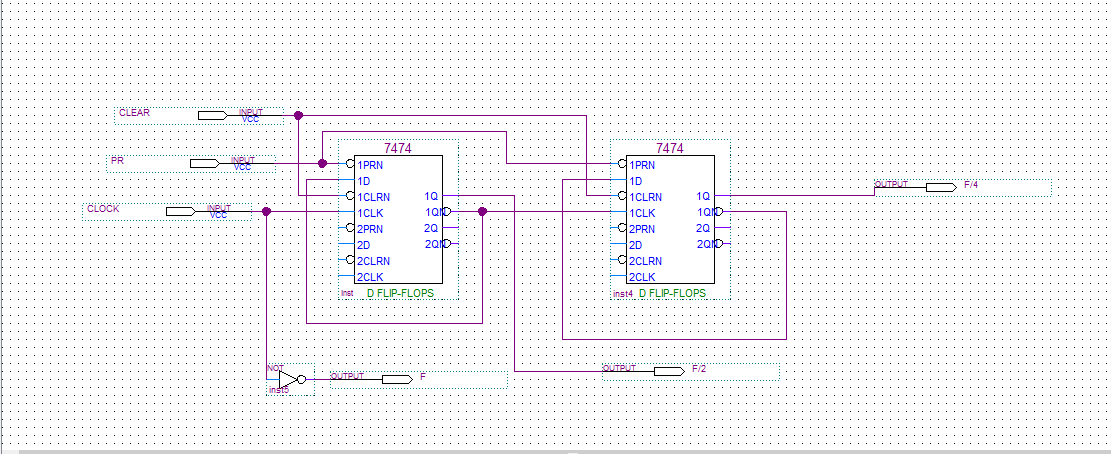
1. **D –Flip –Flop**



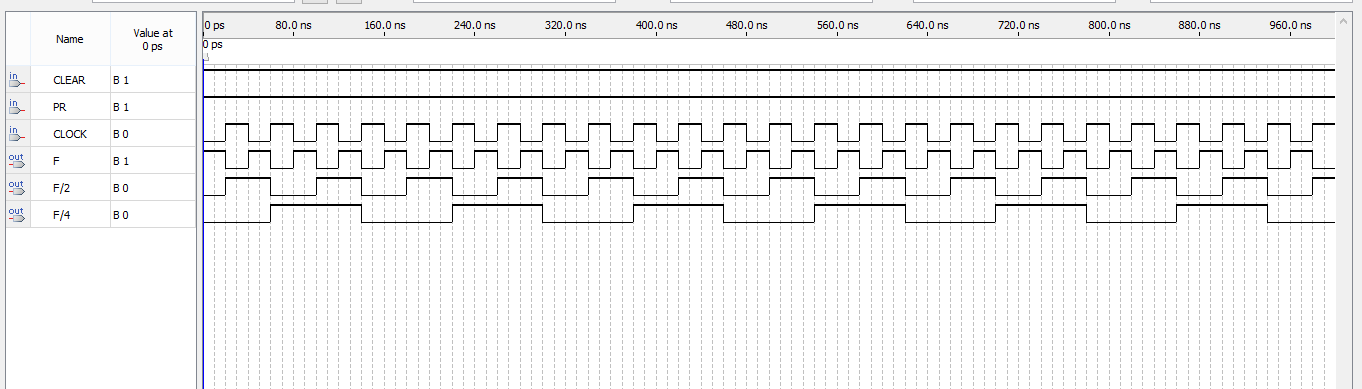
**a) Truth Table**

|  |  |  |  |
| --- | --- | --- | --- |
|  | **C** | **F/2** | **F/4** |
| **c1** | **0** | **0** | **0** |
| **c2** | **1** | **1** | **0** |
| **c3** | **0** | **1** | **0** |
| **c4** | **1** | **0** | **1** |
| **c5** | **0** | **0** | **1** |
| **c6** | **1** | **1** | **1** |
| **c7** | **0** | **1** | **1** |
| **c8** | **1** | **0** | **0** |
| **c9** | **0** | **0** | **0** |
| **c10** | **1** | **1** | **0** |
| **c11** | **0** | **1** | **0** |

**b) Logic Diagram**



**c) Waveform**

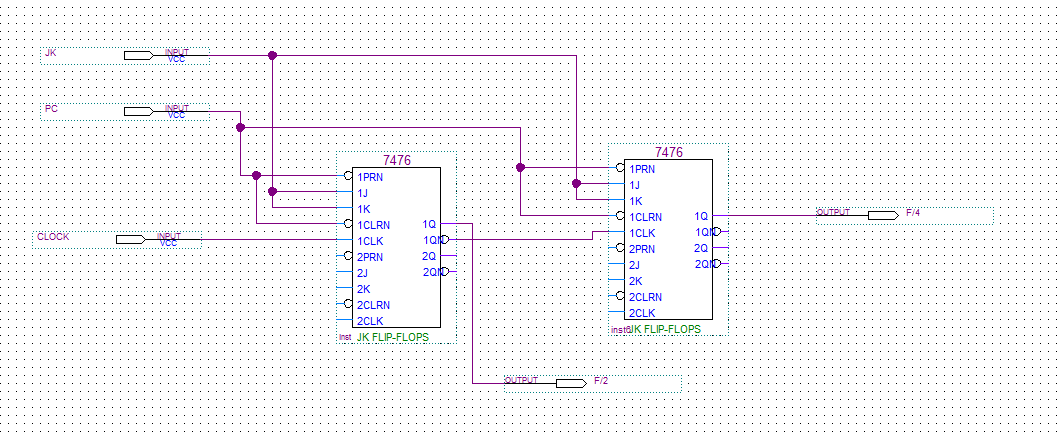
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1. **JK-Flip-Flop**

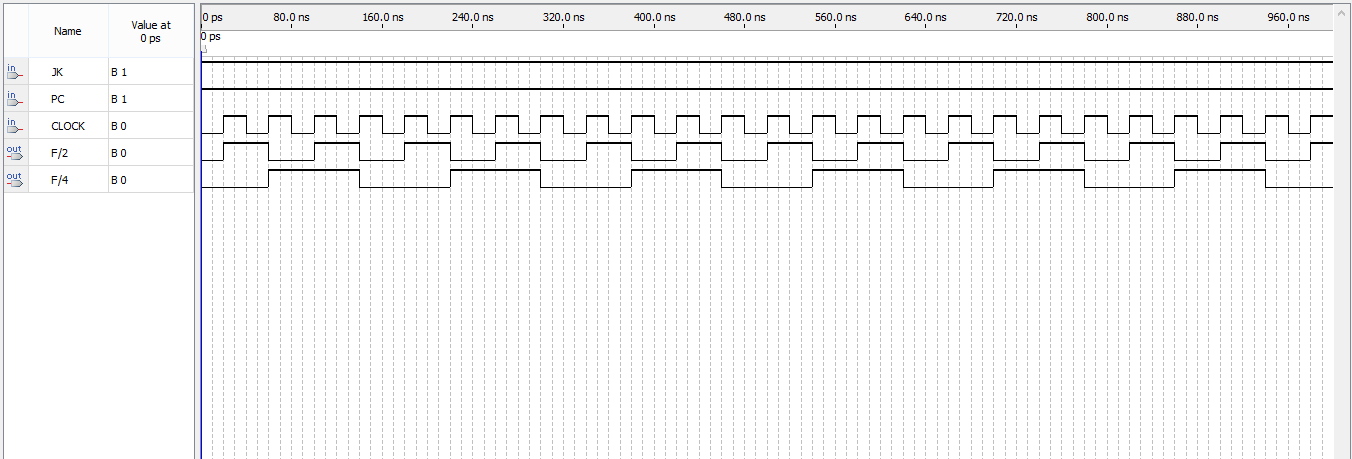
**a) Truth Table**

|  |  |  |  |
| --- | --- | --- | --- |
|  | **C** | **F/2** | **F/4** |
| **c1** | **0** | **0** | **0** |
| **c2** | **1** | **1** | **0** |
| **c3** | **0** | **1** | **0** |
| **c4** | **1** | **0** | **1** |
| **c5** | **0** | **0** | **1** |
| **c6** | **1** | **1** | **1** |
| **c7** | **0** | **1** | **1** |
| **c8** | **1** | **0** | **0** |
| **c9** | **0** | **0** | **0** |
| **c10** | **1** | **1** | **0** |
| **c11** | **0** | **1** | **0** |

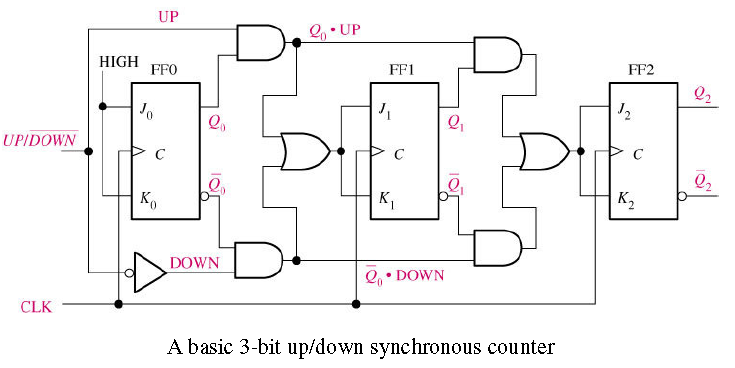
**b) Logic Diagram**

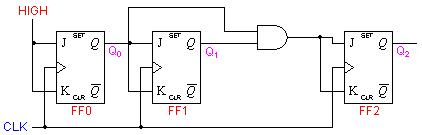


**c) Waveform**

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**Question 2:** 3-bit Synchronous Counter





**a)Truth Table**

**2 ->0->1->5->6**

|  |  |  |
| --- | --- | --- |
| **Q0** | **Q1** | **Q2** |
| **0** | **1** | **0** |
| **0** | **0** | **0** |
| **0** | **0** | **1** |
| **1** | **0** | **1** |
| **1** | **1** | **0** |

|  |  |  |
| --- | --- | --- |
| **Q0+** | **Q1+** | **Q2+** |
| **0** | **0** | **0** |
| **0** | **0** | **1** |
| **1** | **0** | **1** |
| **1** | **1** | **0** |
| **0** | **1** | **0** |

**b)** **Karnaugh Maps**

|  |  |  |  |
| --- | --- | --- | --- |
|  | | Q2 | |
| Q0 | Q1 | 0 | 1 |
| 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | X |
| 1 | 1 | X | X |
| 1 | 0 | X | X |

|  |  |  |  |
| --- | --- | --- | --- |
|  | | Q2 | |
| Q0 | Q1 | 0 | 1 |
| 0 | 0 | 0 | 0 |
| 0 | 1 | X | X |
| 1 | 1 | X | X |
| 1 | 0 | X | 1 |

**J0=Q2. J1=Q0.**

|  |  |  |  |
| --- | --- | --- | --- |
|  | | Q2 | |
| Q0 | Q1 | 0 | 1 |
| 0 | 0 | X | X |
| 0 | 1 | X | X |
| 1 | 1 | 1 | X |
| 1 | 0 | X | 0 |

|  |  |  |  |
| --- | --- | --- | --- |
|  | | Q2 | |
| Q0 | Q1 | 0 | 1 |
| 0 | 0 | 1 | X |
| 0 | 1 | 0 | X |
| 1 | 1 | 0 | X |
| 1 | 0 | X | X |

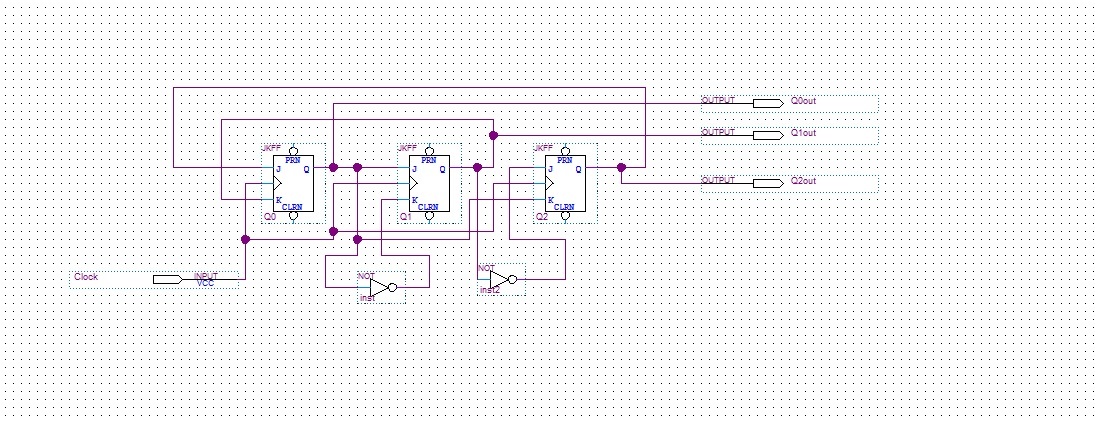
**J2=Q1’ K0=Q1**

|  |  |  |  |
| --- | --- | --- | --- |
|  | | Q2 | |
| Q0 | Q1 | 0 | 1 |
| 0 | 0 | X | X |
| 0 | 1 | 1 | X |
| 1 | 1 | 0 | X |
| 1 | 0 | X | X |

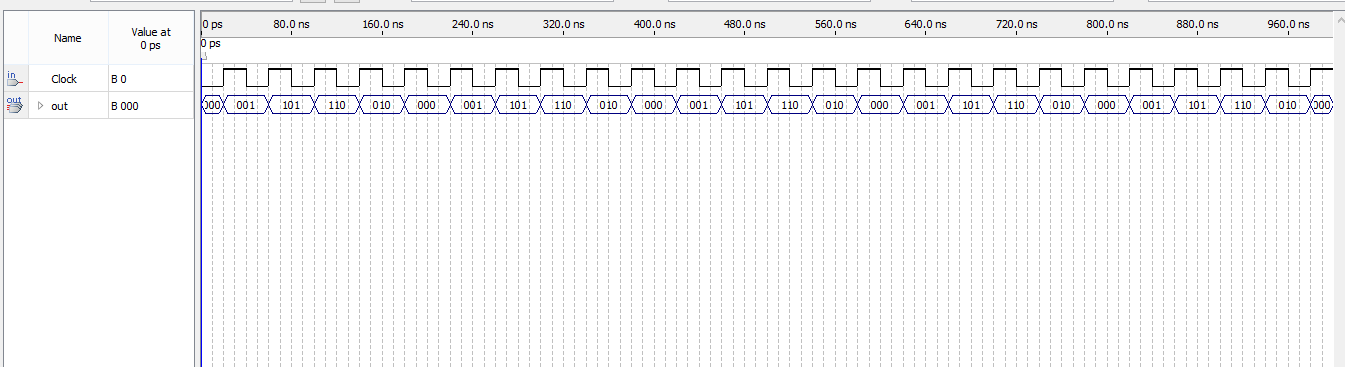
|  |  |  |  |
| --- | --- | --- | --- |
|  | | Q2 | |
| Q0 | Q1 | 0 | 1 |
| 0 | 0 | X | 0 |
| 0 | 1 | X | X |
| 1 | 1 | X | X |
| 1 | 0 | X | 1 |

**K1=Q0’ K2=Q0**

**C)Logic Diagram**



**d)** **Waveform**



**e) VHDL CODE \*** **http://www.tek-tips.com/viewthread.cfm?qid=1232988**

**library    ieee;  
use ieee.std\_logic\_1164.all;  
use ieee.std\_logic\_unsigned.all;  
  
entity BinCount3bit is  
port(  
    clk    : in std\_logic;  
    reset  : in std\_logic;  
    sel    : in std\_logic;  
    q      : out std\_logic\_vector(2 downto 0)  
end BinCount3bit;  
  
architecture behavioral of BinCount3bit is  
begin  
  
process(clk,reset)  
begin  
if reset = '1' then  
  q <= (others => '0');  
elsif(rising\_edge(clk))then  
   if sel = '0' then  
       q <= q+1;  
   else  
       q <= q+2;  
   end if;  
end if;  
end process;  
  
end behavioral;**

